WHAT IS CLAIMED IS:

1. A method of recovering data from a data signal comprising:

receiving a clock signal having a first clock frequency, and alternating between a first level and a second level;

receiving the data signal having a first data rate, the first data rate being substantially equal to the first clock frequency;

providing a first signal by storing the data signal when the clock signal alternates from the first level to the second level;

providing a second signal by passing the first signal when the clock signal is at the first level, and storing the first signal when the clock signal is at the second level;

providing a third signal by delaying the data signal an amount of time;

providing an error signal by combining the first signal and the third signal; and

providing a reference signal by combining the first signal and the second signal.

2. The method of claim 1 further comprising:

applying the error signal and the reference signal to a loop filter to generate a loop filter output.

3. The method of claim 1 wherein first signal is provided by a flip-flop, and the second signal is provided by a latch.

4. The method of claim 3 wherein the providing an error signal and providing a reference signal are done by exclusive-OR gates.

5. The method of claim 3 wherein the delay is approximately equal to a clock-to-Q delay of the flip-flop.

6. The method of claim 5 wherein the flip-flop and the latch have inductors as loads.

7. A phase detector for recovering data from a data signal comprising:

a first storage device configured to receive and store the data signal and to generate a first signal;

a second storage device configured to receive and store the first signal and to generate a second signal;

a delay block configured to receive and delay the data signal and to generate a third signal;

a first logic circuit configured to combine the first and second signals; and

a second logic circuit configured to combine the first and third signals.

8. The phase detector of claim 7 wherein the first storage device is a flip-flop and the second storage device is a latch.

9. The phase detector of claim 8 wherein the flip-flop and the latch receive a clock signal, the clock signal having first edges from a first level to a second level and second edges from the second level to the first level.

10. The phase detector of claim 9 wherein the flip-flop stores the received data signal on the first edges of the clock and the latch latches the first signal when the clock is at the second level.

11. The phase detector of claim 10 wherein the first edges are falling edges and the second edges are rising edges.

12. The phase detector of claim 8 wherein a delay through the delay block is approximately equal to a clock-to-Q delay of the flip-flop.

13. A phase detector for recovering data from a received data signal comprising:

a flip-flop having a data input coupled to a data input port, and a clock input coupled to a clock port;

a latch having a data input coupled an output of the first flip-flop, and a clock input coupled to the clock port;

a delay element having an input coupled to the data input port;

a first logic circuit having a first input coupled to the output of the flip-flop and a second input coupled to an output of the latch; and

a second logic circuit having a first input coupled to the output of the first flip-flop and a second input coupled to an output of the delay element.

14. The phase detector of claim 13 wherein the first data input port is configured to receive a differential signal.

15. The phase detector of claim 14 wherein the first clock port is configured to receive a differential signal.

16. The phase detector of claim 15 wherein the first logic circuit and the second logic circuit are exclusive-OR gates.

17. The phase detector of claim 15 wherein the first logic circuit and the second logic circuit perform an exclusive-OR function.

18. The phase detector of claim 13 wherein the first logic circuit provides a reference signal, and the second logic circuit provides an error signal.

19. An optical receiver comprising the phase detector of claim 13.

20. An optical transceiver comprising:
an optical transmitter; and
the optical receiver of claim 19 coupled to the optical transmitter.

21. A system for receiving and transmitting optical signals comprising:
a light emitting diode, configured to transmit optical signals;
a transmitter coupled to the light emitting diode;
a photo-diode, configured to receive optical signals;
a receive amplifier coupled to the photo-diode; and
the phase detector of claim 13 coupled to the receive amplifier.

22. The phase detector of claim 13 wherein the latch comprises:
first and second MOSFETs having their source terminals connected together, their gate terminals coupled to receive a pair of logic signals, respectively, and their drain terminals connected to a true output and a complementary output, respectively;

a first clocked MOSFET having a drain terminal coupled to the source terminals of the first and second MOSFETs, a gate terminal coupled to receive a first clock signal, and a source terminal;

third and fourth MOSFETs having their source terminals coupled together, their gate terminals and drain terminals respectively cross-coupled to the true output and the complementary output;

a second clocked MOSFET having a drain terminal coupled to the source terminals of the third and fourth MOSFETs, a gate terminal coupled to receive a second clock signal, and a source terminal;

a first load including a resistive element and an inductive element connected in series and coupling the true output to a first power supply terminal;

a second load including a resistive element and an inductive element connected in series and coupling the true output to the first power supply terminal; and

a current-source MOSFET coupled between the source terminals of the first and second clocked MOSFETs and a second power supply terminal.

23. The phase detector of claim 22 wherein the flip-flop comprises:

a first clocked latch as set forth in claim 22; and

a second clocked latch as set forth in claim 22,

wherein, the gate terminals of the first and second MOSFETs in the second clocked latch respectively couple to the true output and the complementary output of the first clocked latch.